

1 **51358/SDB/B600**

ABSTRACT OF THE DISCLOSURE

5 Methods and circuitry for implementing high speed first-
in first-out (FIFO) structures. In one embodiment, a FIFO is
disclosed that allows the frequency of one clock, e.g., the
write clock, to be different than (e.g., half) that of the
other (read) clock. In another embodiment a FIFO is presented
that can be set and/or reset asynchronously. Other
10 embodiments are disclosed wherein the read and write pointers
are effectively monitored to ensure proper timing
relationship, to detect loss of clock as well as to detect
other abnormal FIFO conditions.

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